

Amendments to the Claims:

A listing of the entire set of pending claims (including amendments to the claims, if any) is submitted herewith per 37 CFR 1.121. This listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Previously Presented) A digital signal processing apparatus for executing a plurality of operations comprising:

a plurality of functional units wherein each functional unit is adapted to execute operations, and

control means for controlling the functional units,

the control means includes:

a fetch unit, a decode unit, and

a plurality of control units responsive to the decode unit,

wherein

each functional unit has a corresponding control unit of the plurality of control units for controlling a function of the functional unit defined by one or more operations from the decode unit, including controlling a number of repetitions of execution of the function, and

each functional unit is adapted to execute the operations for the number of repetitions in an autonomous manner under control of the control unit associated with the functional unit.

2. (Currently Amended) An apparatus according to claim 1, characterized by further comprising FIFO (first-in/first-out) register means adapted for supporting data-flow communication among said functional units.

3. (Currently Amended) A digital signal processing apparatus for executing a plurality of operations, comprising a plurality of functional units wherein each functional unit is adapted to execute operations, and respective private control means for each functional unit for controlling the functional unit in coordination with one another, characterized by FIFO (first-in/first-out) registers adapted for supporting data-flow communication among the functional units, wherein execution of the operations at the functional units is dependent at least in part on ~~the a~~ state of the registers.

4 (Canceled)

5. (Currently Amended) An apparatus according to claim 2, ~~characterized in that wherein~~ said FIFO register means comprises a plurality of FIFO registers.

6. (Currently Amended) An apparatus according to claim 1, ~~characterized in that wherein~~ each of said functional units are provided with at least one control unit.

7. (Currently Amended) An apparatus according to claim 1, ~~which wherein the~~ apparatus is adapted to execute a pipeline consisting of a plurality of stages, wherein each stage is executed by a corresponding functional unit.

8. (Currently Amended) An apparatus according to claim 1, ~~characterized in that wherein~~ for each control unit an instruction register and a counter are provided, wherein said counter indicates ~~the a~~ number of times an instruction stored in said instruction register has to be executed by the corresponding functional unit.

9. (Previously Presented) An apparatus according to claim 1, further comprising a program memory means storing a main program, characterized in that said main program contains directives for instructing said control units.

10. (Currently Amended) A method for processing digital signals in a digital signal processing apparatus, comprising a plurality of functional units wherein each functional unit is adapted to execute operations, ~~characterized in that wherein~~ the functional units are controlled by control means including a single fetch unit, a single decode unit and a plurality of private control units wherein each private control unit is operatively associated with a respective functional unit so that each functional unit is able to execute operations in an autonomous manner under control of the private control unit associated therewith, the control unit controlling a number ~~[[or]]~~ of repetitions of execution of its associated functional unit.

11. (Previously Presented) An apparatus according to claim 9, characterized in that data-flow communication among said functional units is supported by FIFO (first-in/first-out) register means.

12 (Canceled)

13. (Previously Presented) An apparatus according to claim 11, wherein a pipeline consisting of a plurality of stages is provided, and each stage is executed by at least one of said functional units.

14. (Currently Amended) An apparatus according to claim 1, ~~characterized in that wherein~~ the number of times an instruction stored has to be executed by at least one of said functional units is counted by the corresponding control unit.

15 (Canceled)

16. (Previously Presented) A digital signal processor comprising:
a plurality of functional units, each functional unit including a local control unit and an execution element;
a fetch unit that is configured to retrieve instructions from a memory; and

a decode unit that is configured to process the instructions to provide a plurality of sets of operations, each set being provided to the local control unit of a corresponding functional unit;

wherein the fetch unit is configured to initiate execution of each set of operations at each corresponding functional unit for a given number of iterations, and

each functional unit is configured to autonomously execute the set of operations for the given number of iterations upon initiation by the fetch unit.

17. (Previously Presented) The processor of claim 16, wherein the sets of operations are configured to selectively include no-operation (nop) elements that facilitate synchronization among the functional units.

18. (Previously Presented) The processor of claim 16, including a plurality of registers, wherein the execution of particular operations at the functional units is dependent upon a state of at least one of the registers.

19. (Previously Presented) The processor of claim 18, wherein the plurality of registers include one or more first-in/first-out registers.

20. (Previously Presented) The processor of claim 16, wherein access to the memory for storing a result of the execution of the set of operations is limited to fewer than all of the functional units.

21. (Previously Presented) The processor of claim 16, wherein each local control unit includes a plurality of registers for storing the set of operations, and a counter for controlling the execution of the set of operations in the registers for the given number of iterations.

22. (Previously Presented) The processor of claim 16, wherein each local control unit signals the fetch unit upon execution of the set of operations in the register for the given number of iterations.